

PG180-A02

256b GDDR6 x16
TALL DP + DP + DP + HDMI/DP + USB

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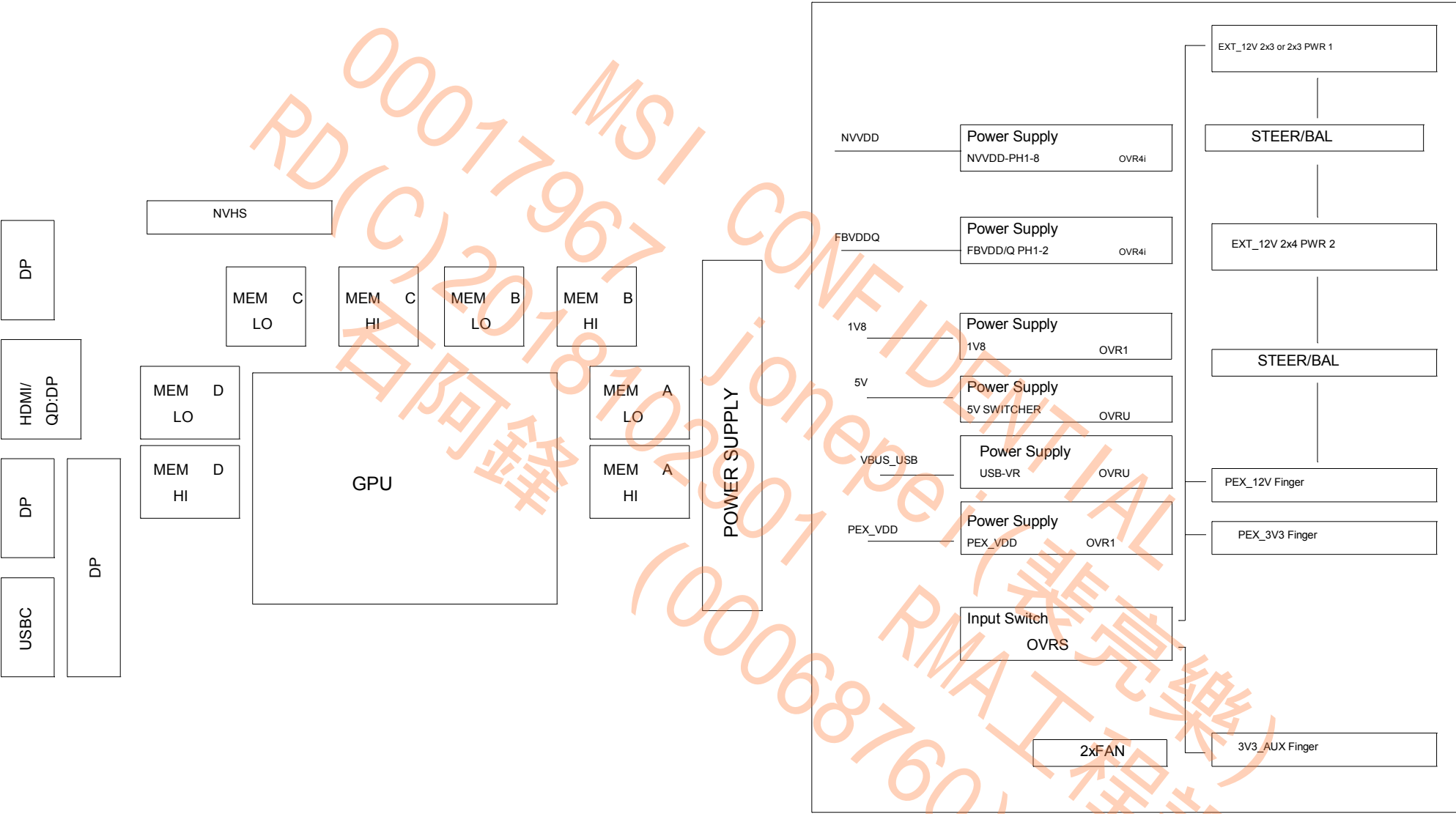
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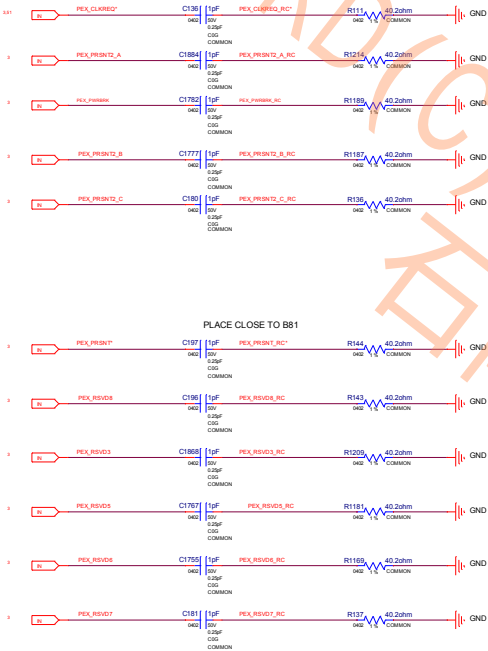
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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	Block Diagram

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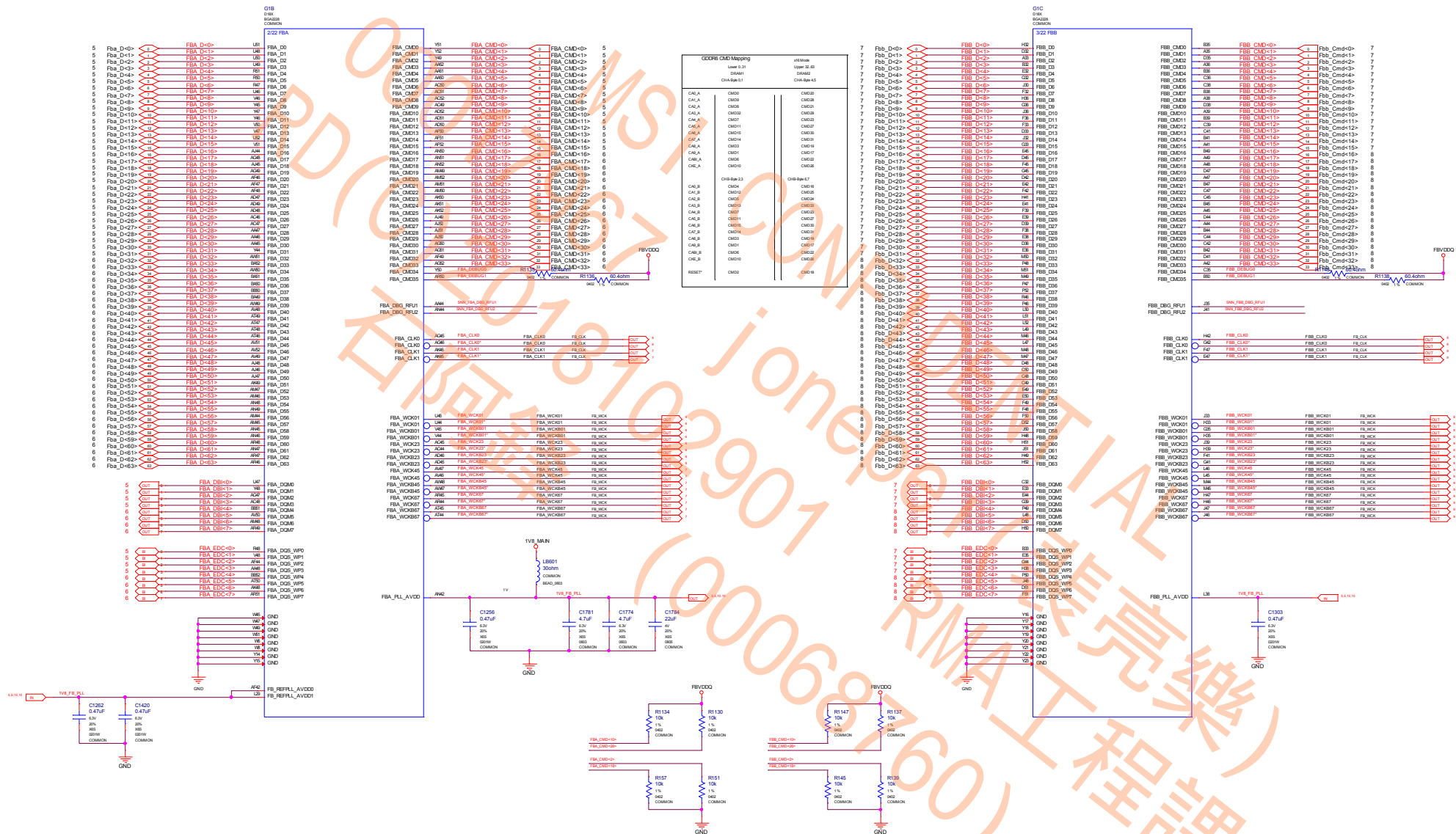
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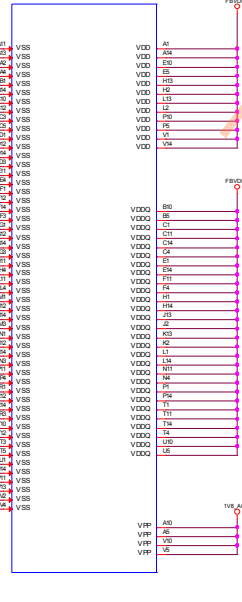
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PAGE:DETAIL	PCI Termination

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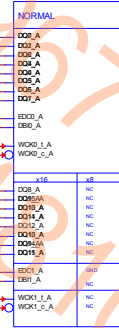




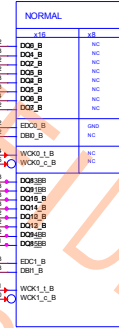
M11D
HYPERMEMORY-HA
FBA-HA
COMMON



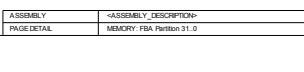
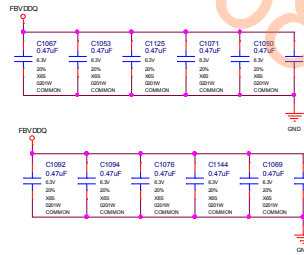
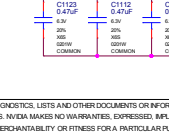
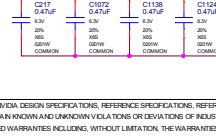
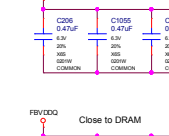
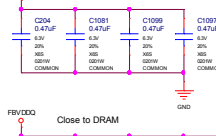
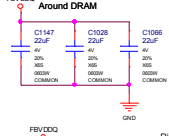
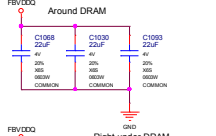
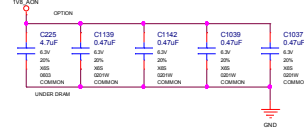
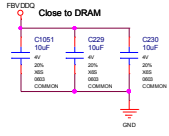
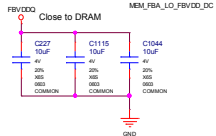
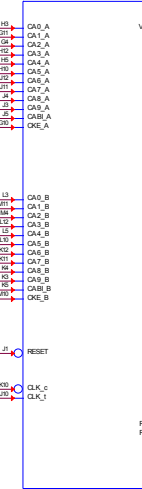
M11A
HYPERMEMORY-HA
FBA-HA
COMMON



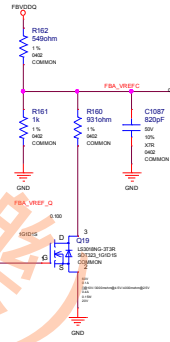
M11B
HYPERMEMORY-HA
FBA-HA
COMMON



M11C
HYPERMEMORY-HA
FBA-HA
COMMON

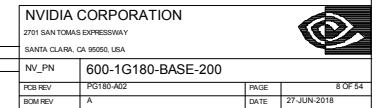


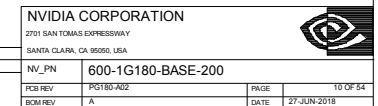
VREFC IS NOT USED IN x16 CONFIGURATION
1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R106

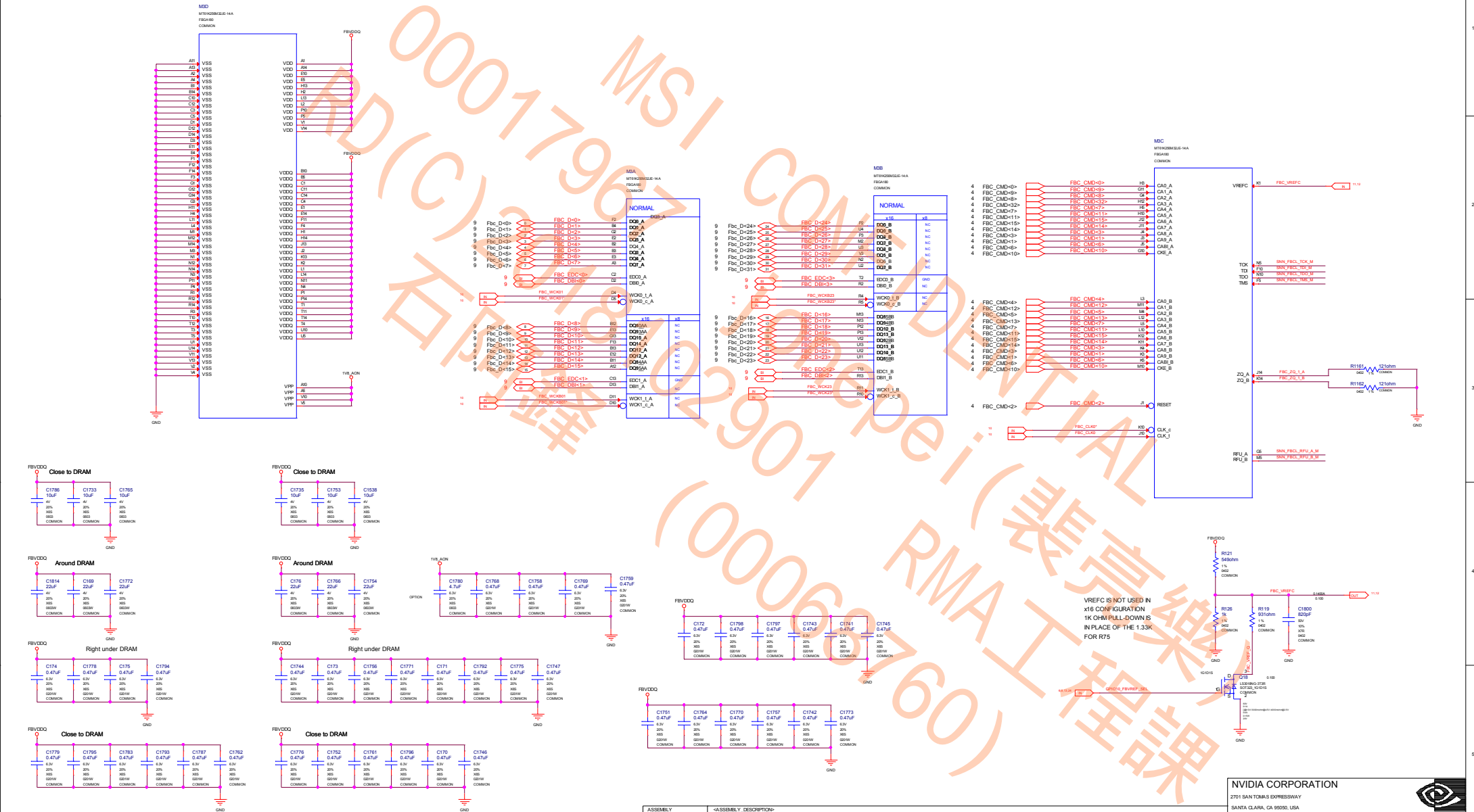


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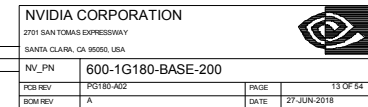
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PAGE DETAIL	MEMORY: FBC Partition 31..0

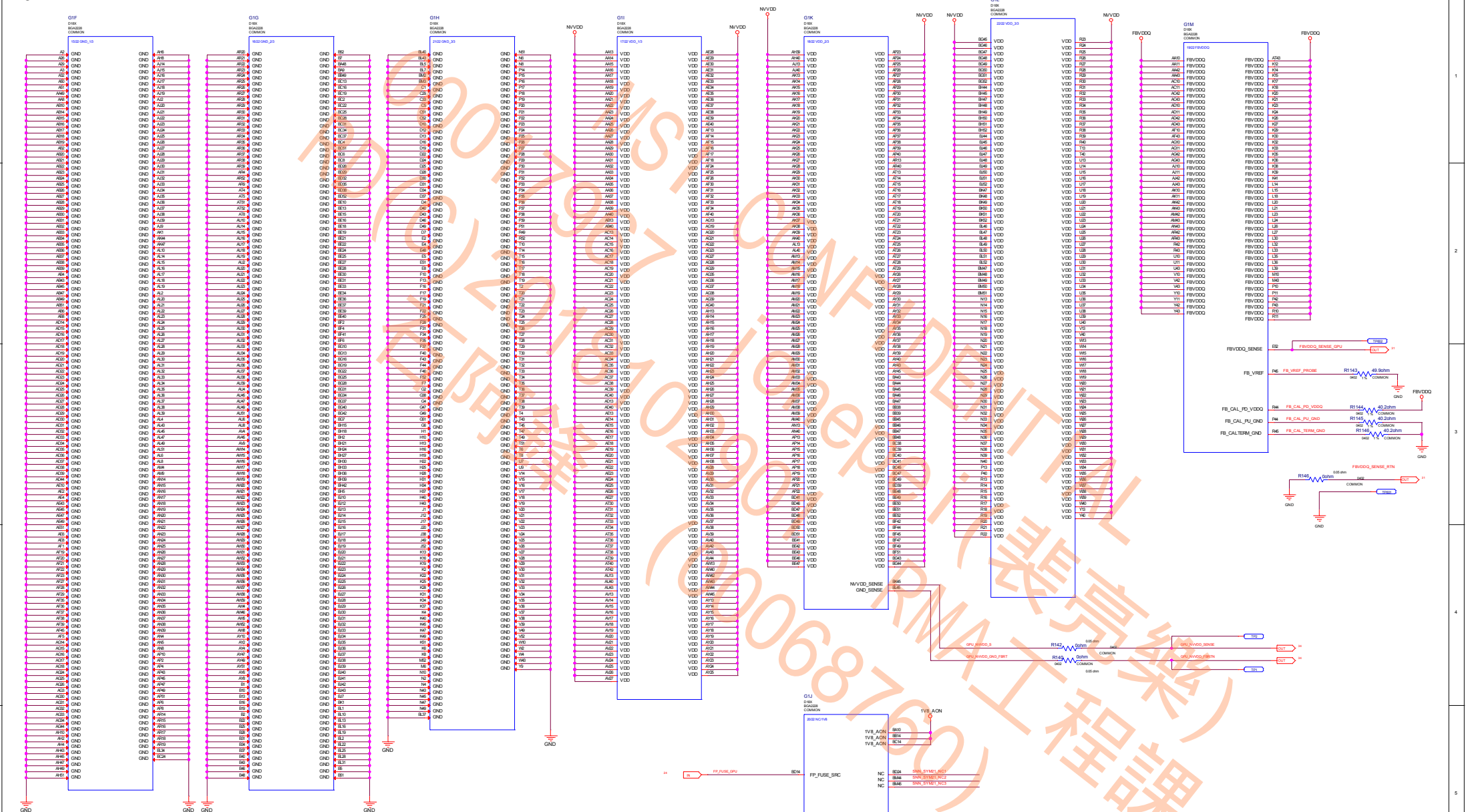
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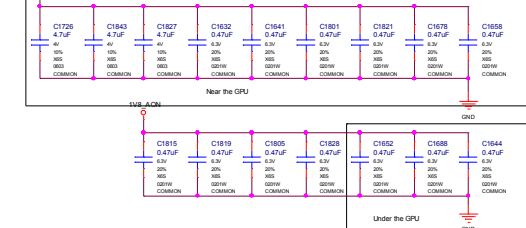


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PAGE DETAIL	GPU PWR and QND	600-1G180-BASE-200	
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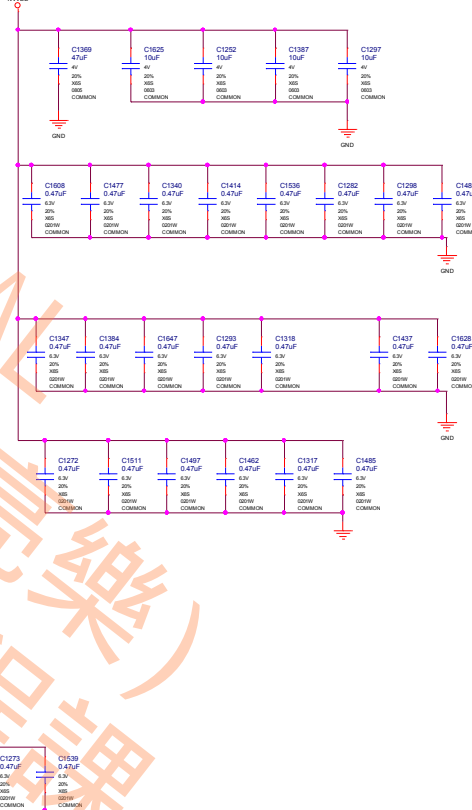
NVDE



1V8_AON



NVVDD



032-0532-000
X6S
0805

0805	
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU Decoupling

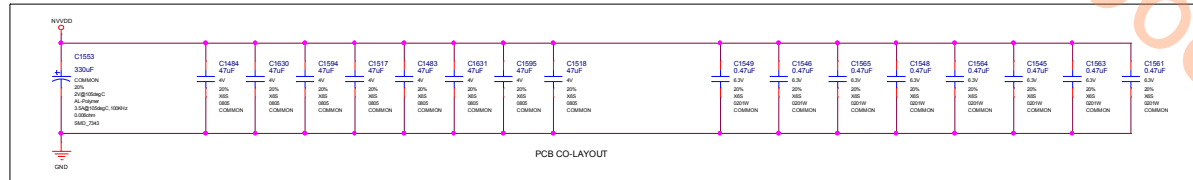
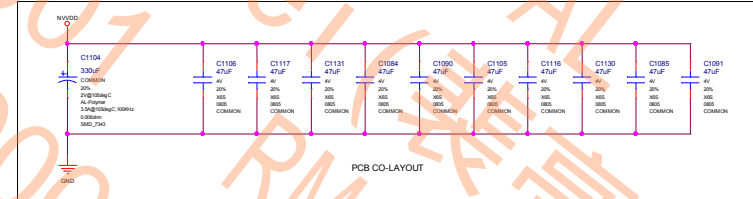
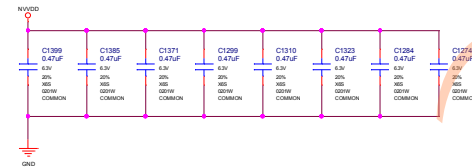
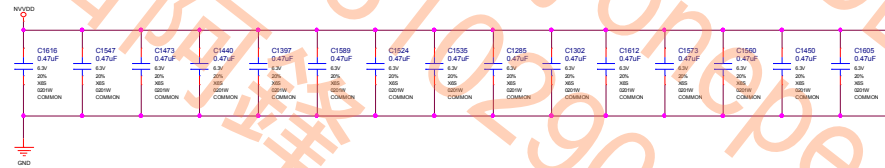
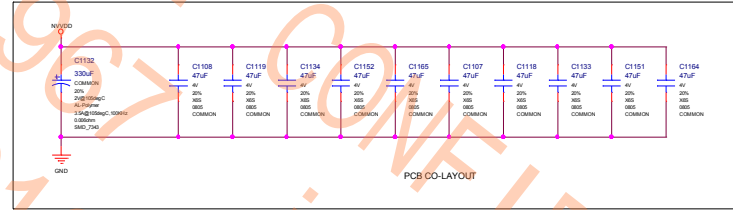
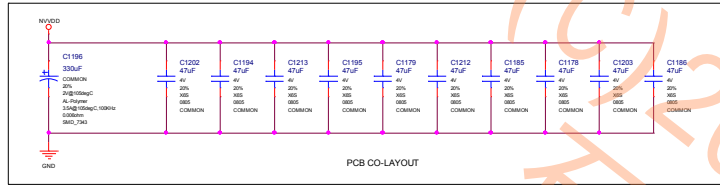
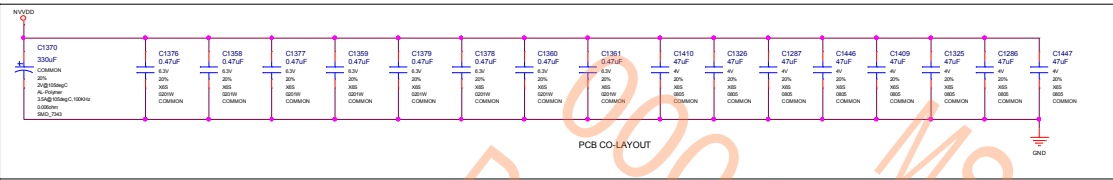
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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	GPU DECOUPLING

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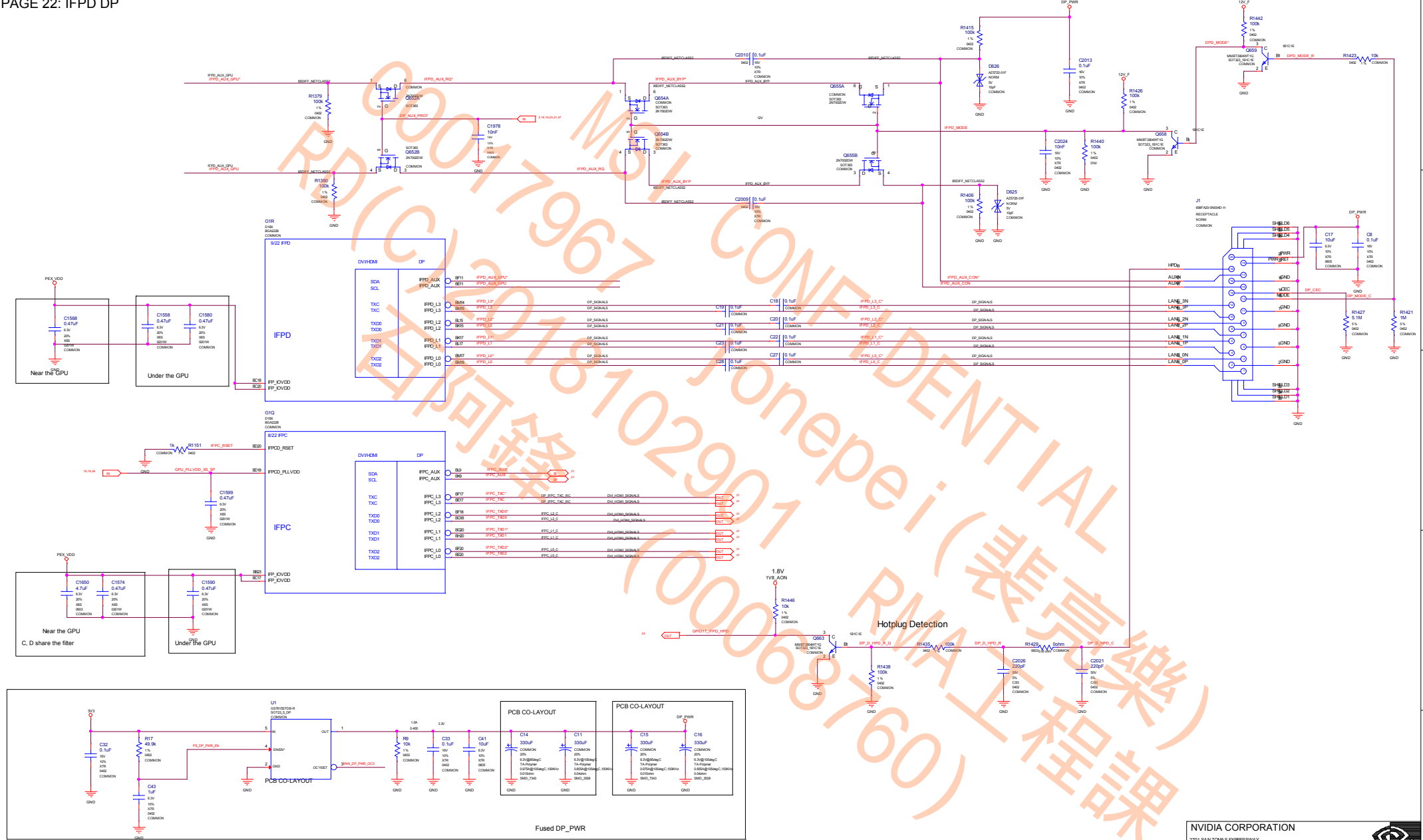


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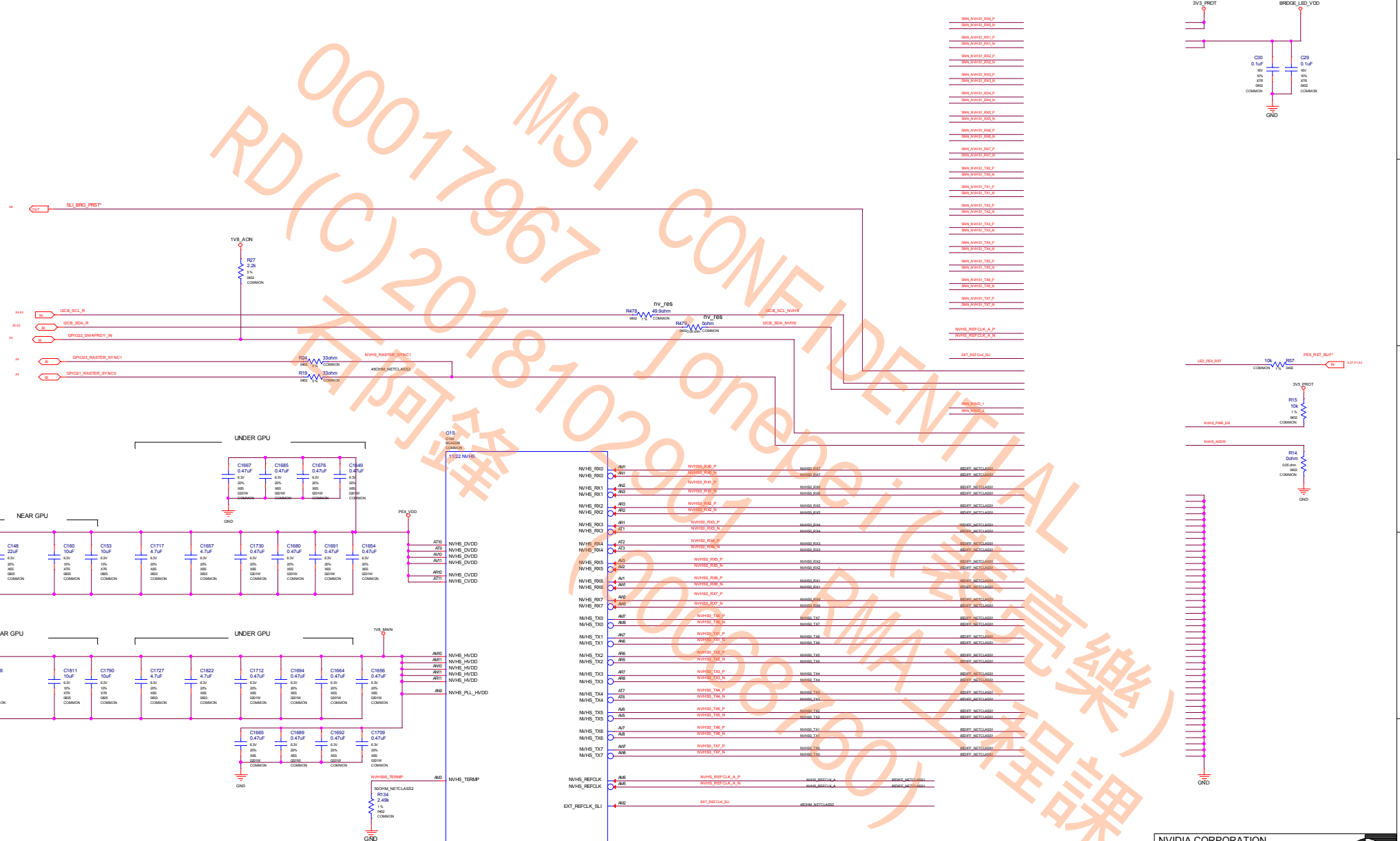




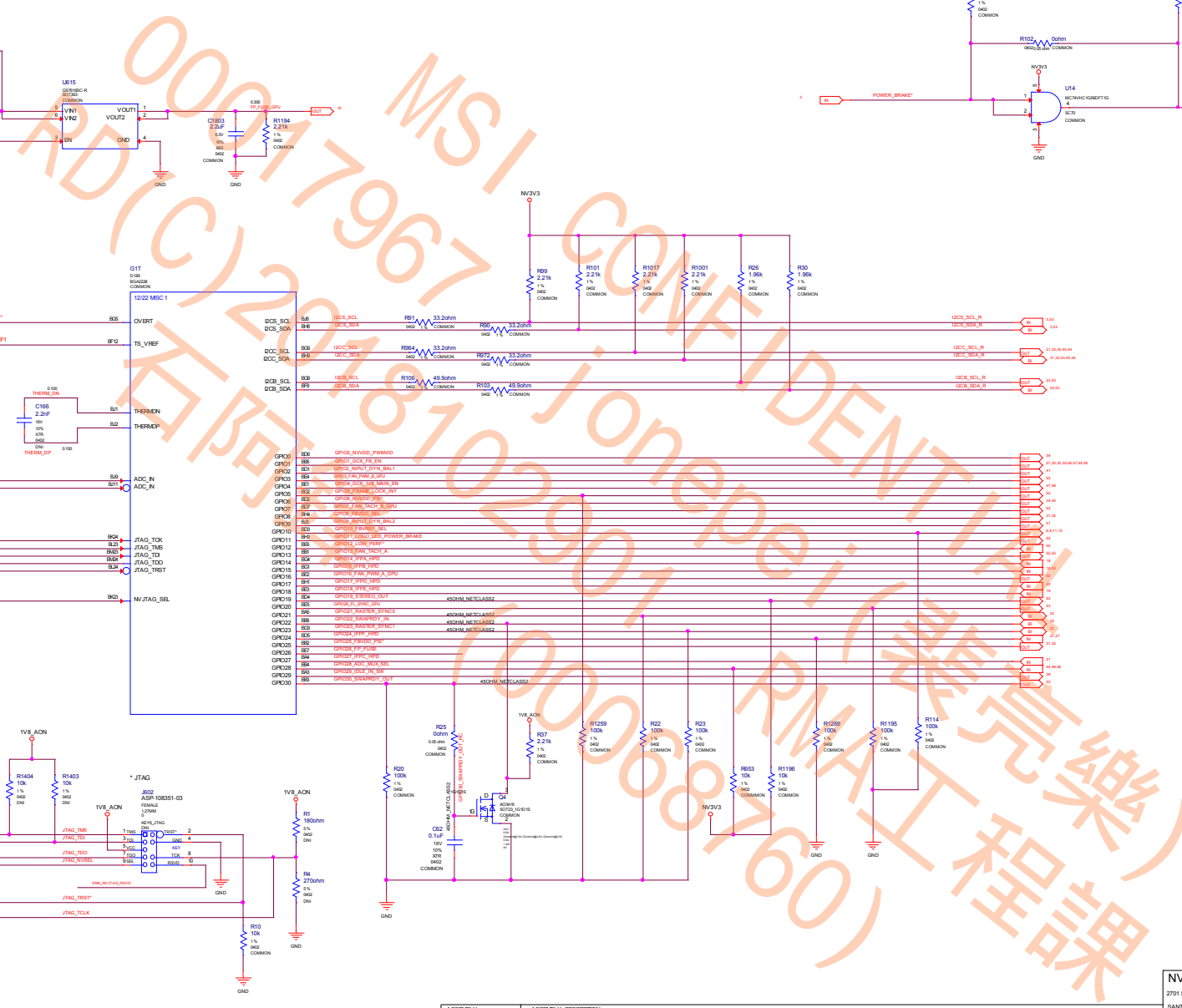
ASSEMBLY		ASSEMBLY DESCRIPTION	
PAGE DETAIL		IFPD DP	

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PAGE DETAIL	NV16 INTERFACE	NV_PN 600-1G180-BASE-200	
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC: FAN,THERMAL,JTAG,GPIO,STEREO

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]	FS_OVERT	
L	L	L	XXX1	1:ENABLE 0:DISABLE	
L	L	M	XXX0	FS_OVERT ENABLE	
L	L	M	XXX0	FS_OVERT DISABLE	

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

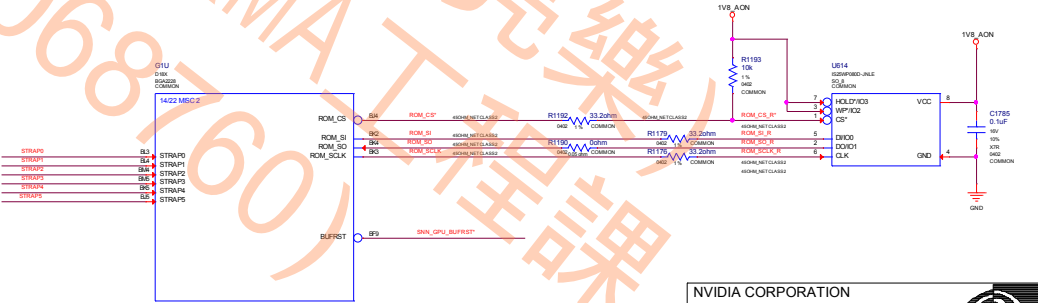
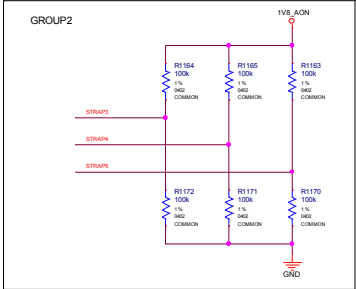
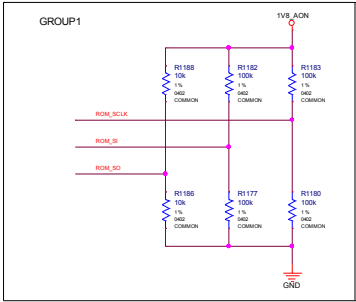
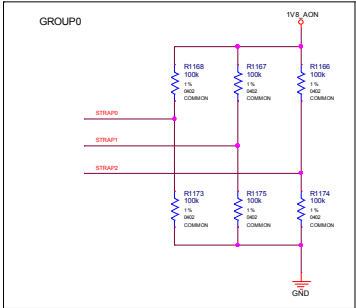
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Default

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung



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ASSEMBLY

ASSEMBLY DESCRIPTION

PAGE:DETAIL

MISC3: ROM STRAPS

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NV_PN

600-1G180-BASE-200

PCB REV

PG180-A02

ROM REV

A

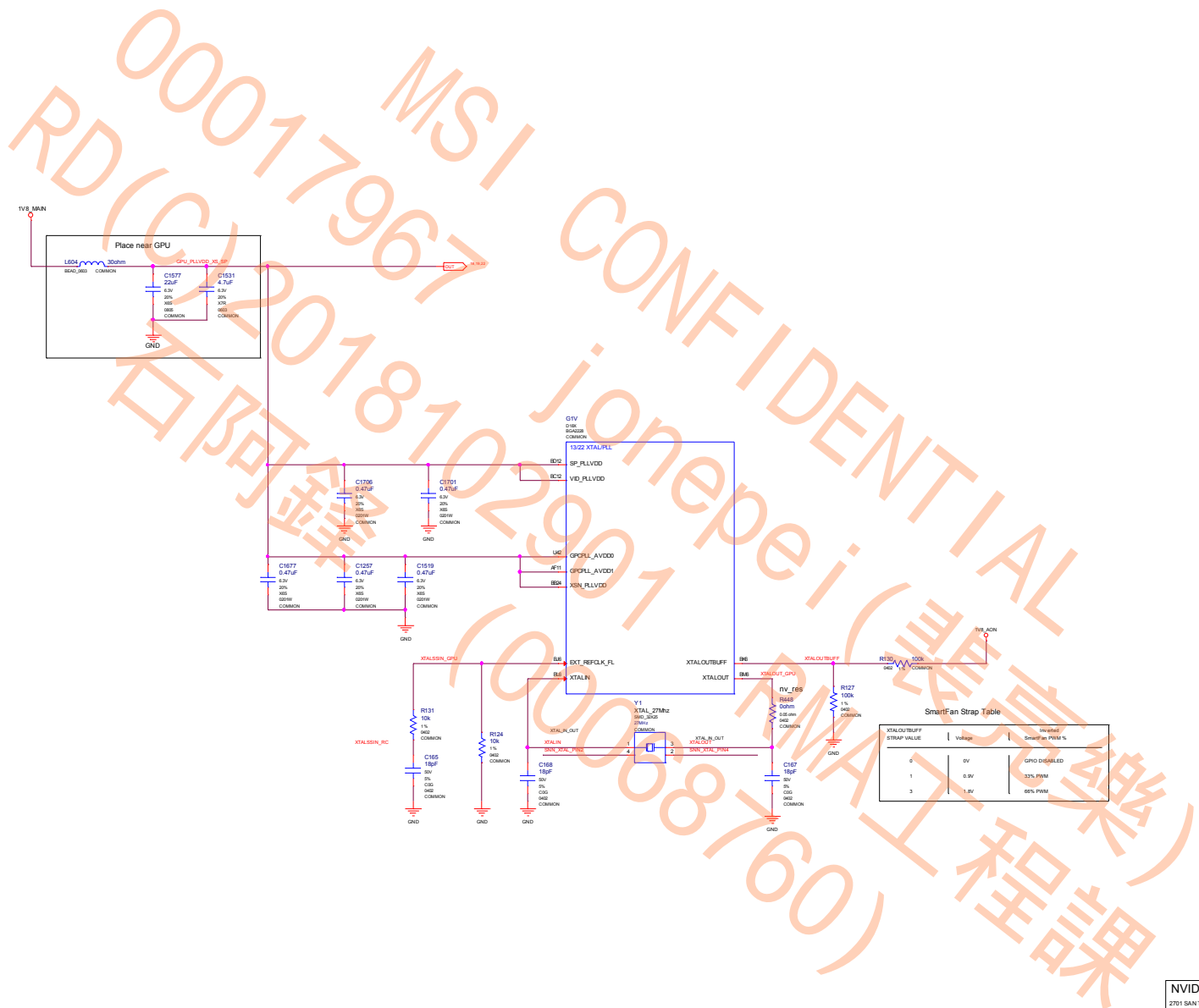
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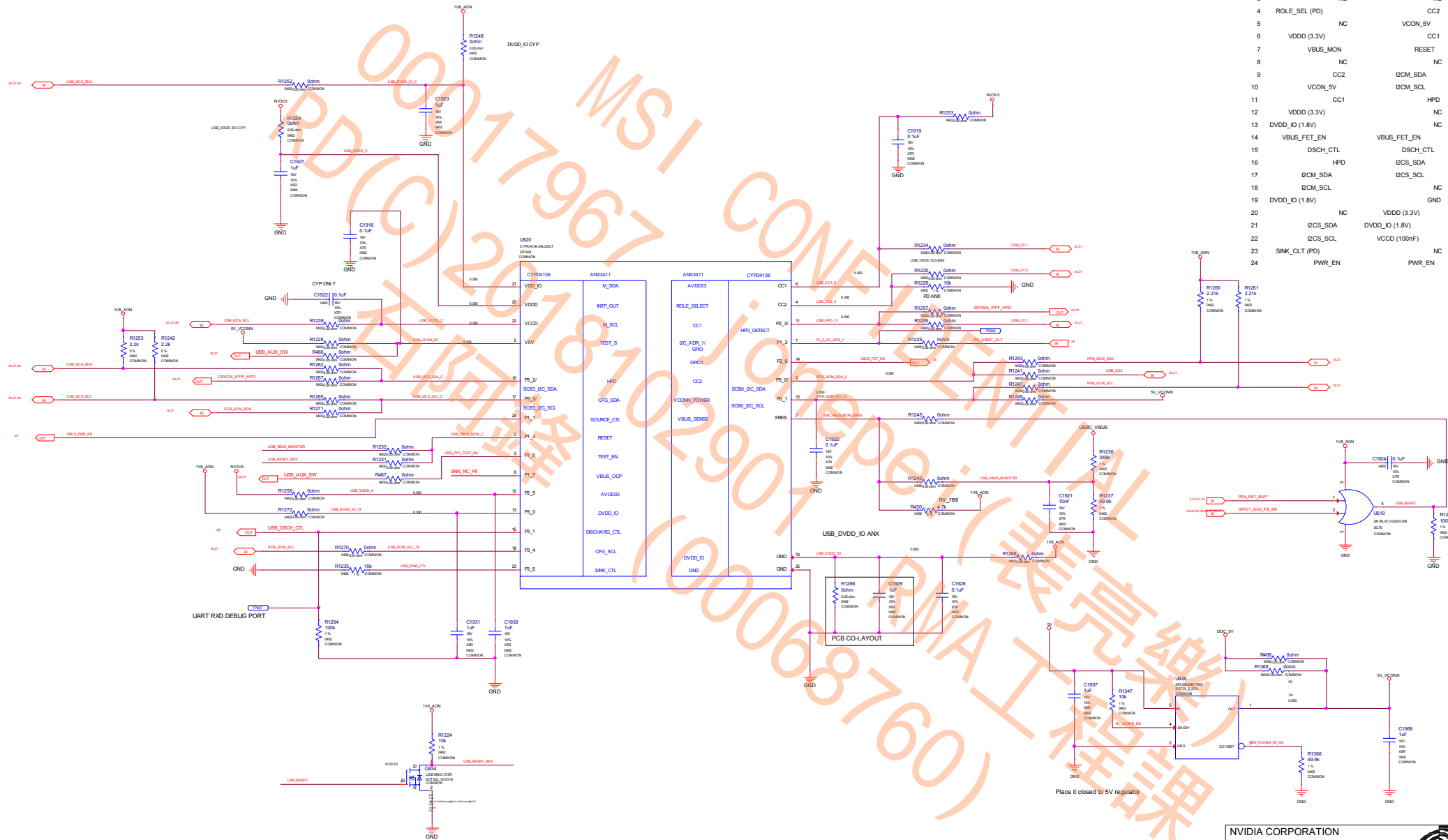


XTALOUTBUFF STRAP VALUE	Voltage	Inverted Search on PWM %
0	0V	GPI0 DISABLE
1	0.9V	33% PWM
3	1.8V	66% PWM

NV_PN	600-1G180-BASE-20
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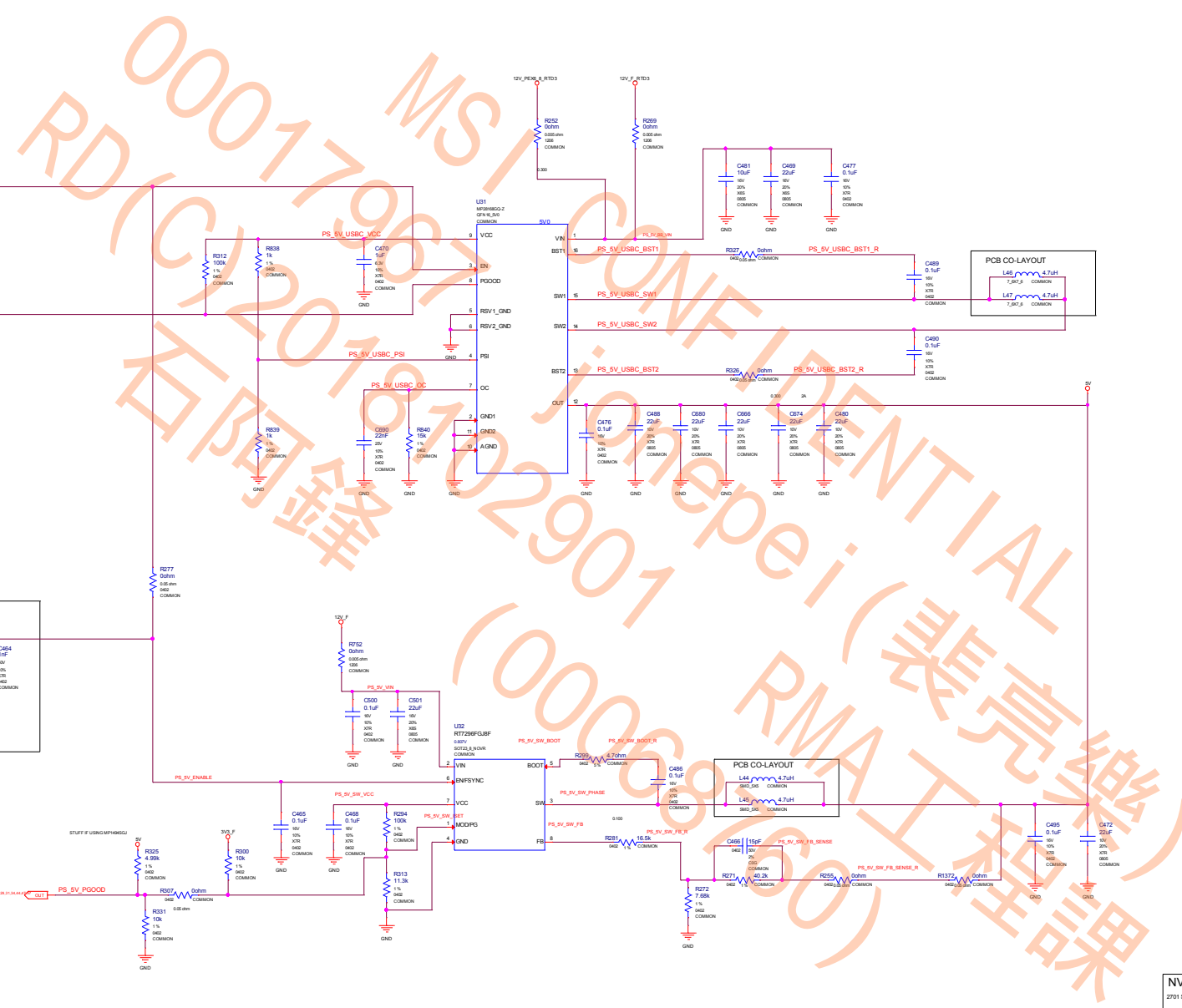
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2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_SV
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_SV	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100nF)
23	SINK_CTL (PD)	NC
24	PWR_EN	PWR_EN

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PCB REV	PG180-A02
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BOM REV	A	DATE	27-JUN-2018
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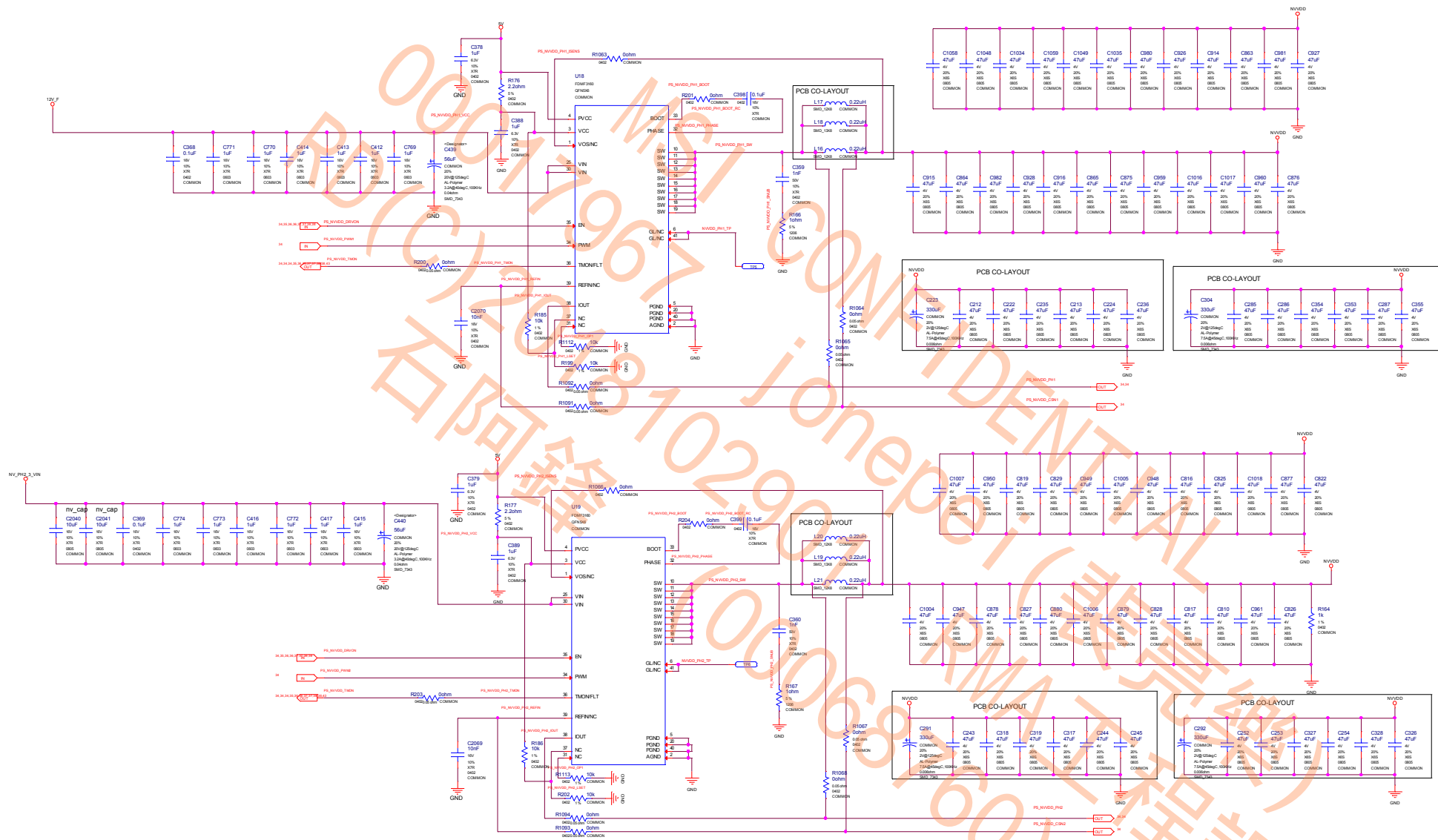
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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	PS: NVVDD Phase 1, 2

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NV_PN 600-1G180-BASE-200

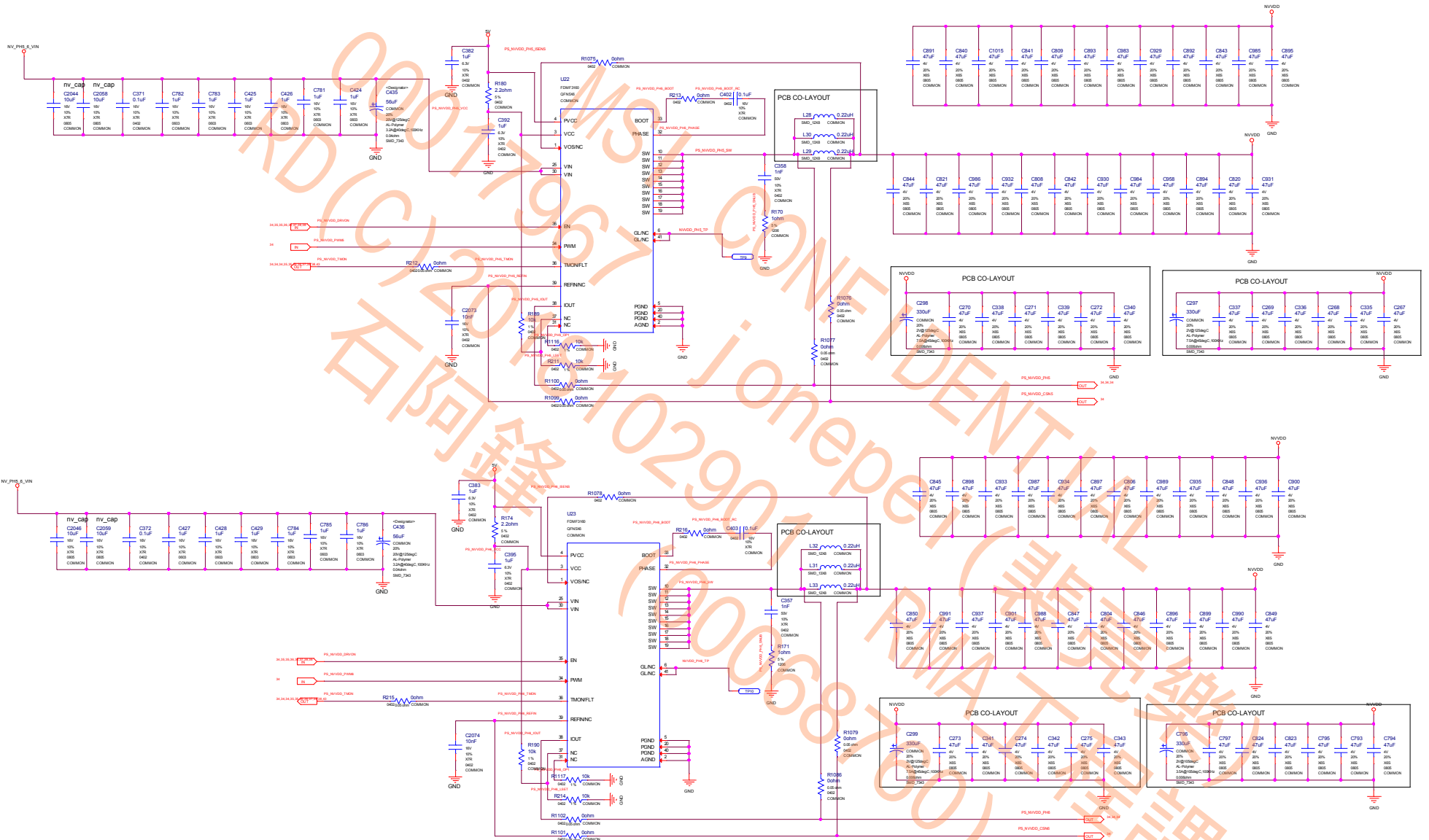
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVDD Phase 3, 4



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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE: 37 OF 54	PS: NVVDD Phase 5, 6

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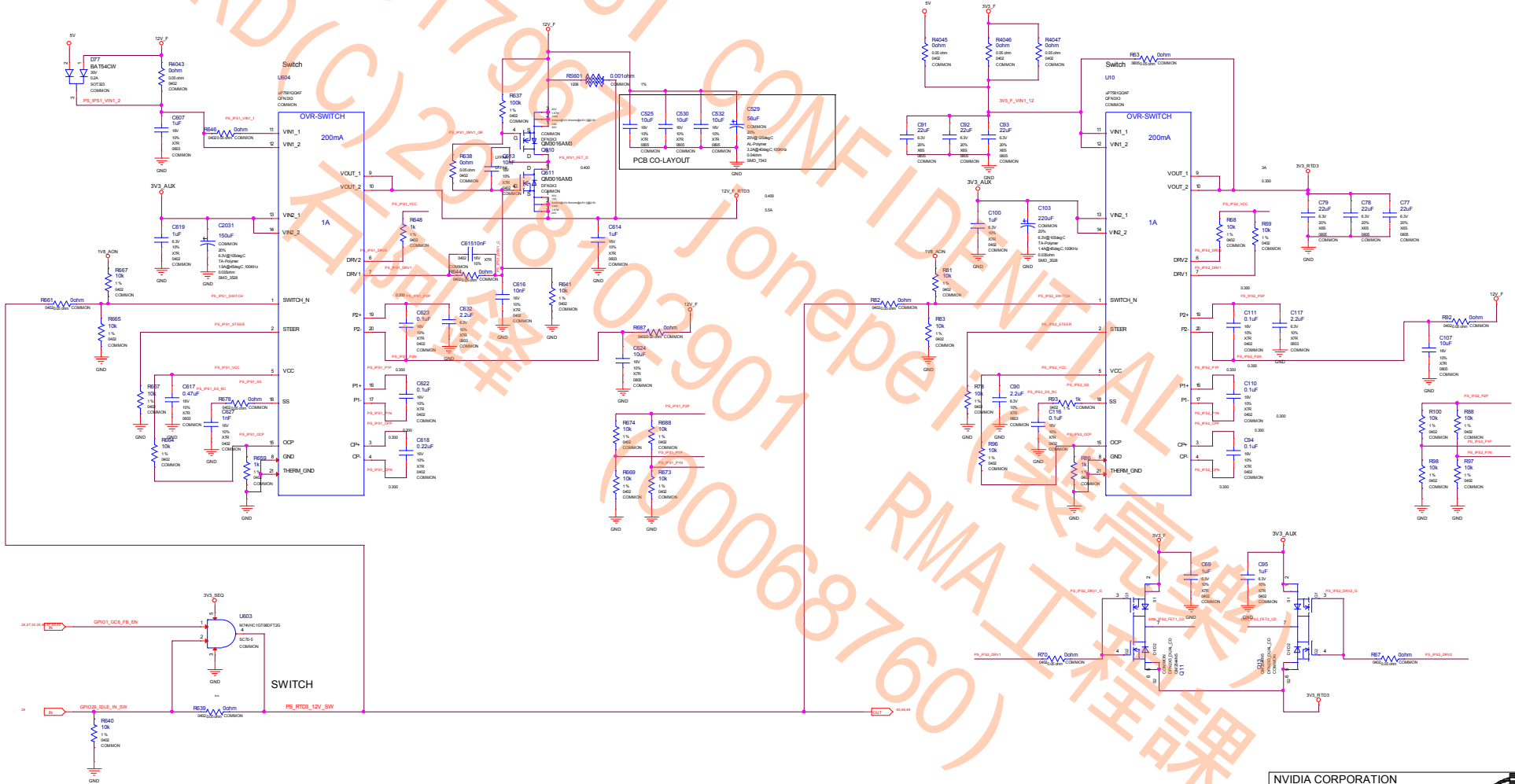
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PAGE DETAIL	PS: NVQCO Phase 7, 8

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A



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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE: 39	PS: INPUT SWITCH RTD3

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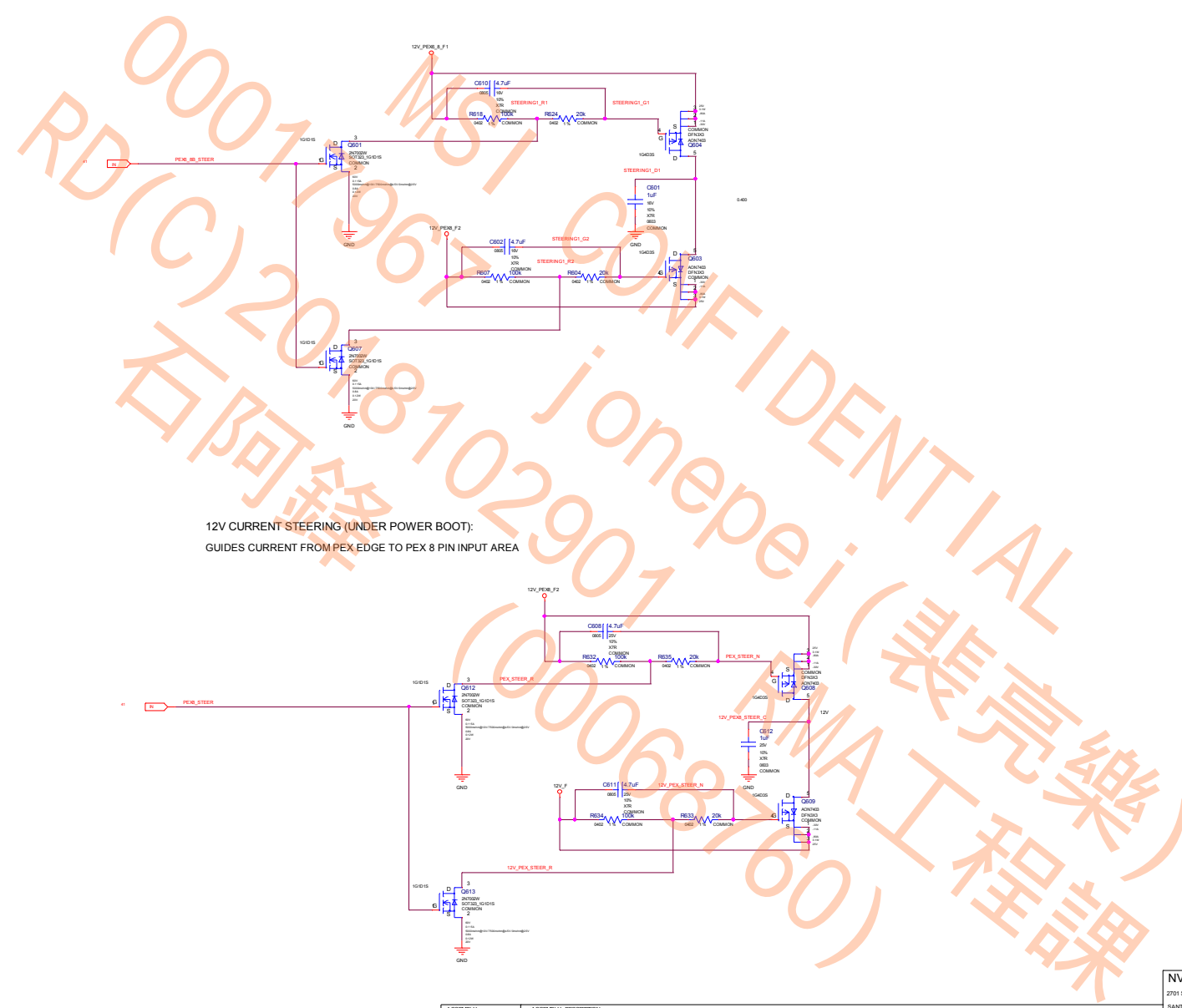
NV_PN 600-1G180-BASE-200

PCB REV PG180-A02
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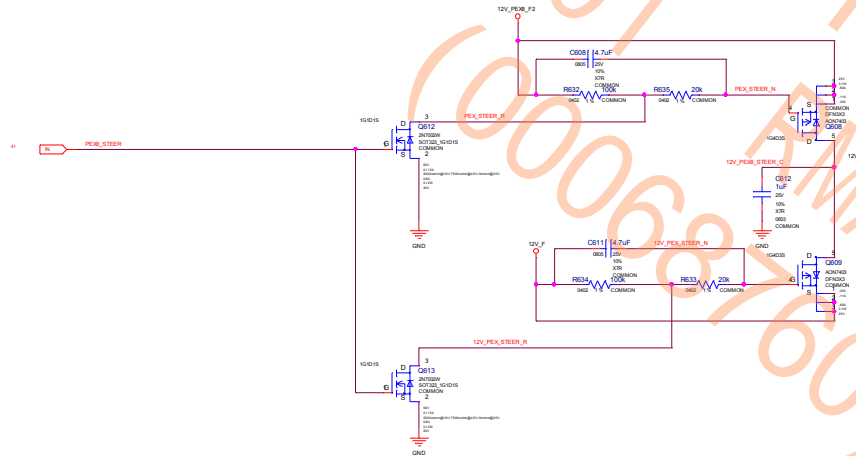
NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN	600-1G180-BASE-200		
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12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



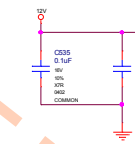
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PAGE DETAIL	PS: 12V CURRENT STEERING


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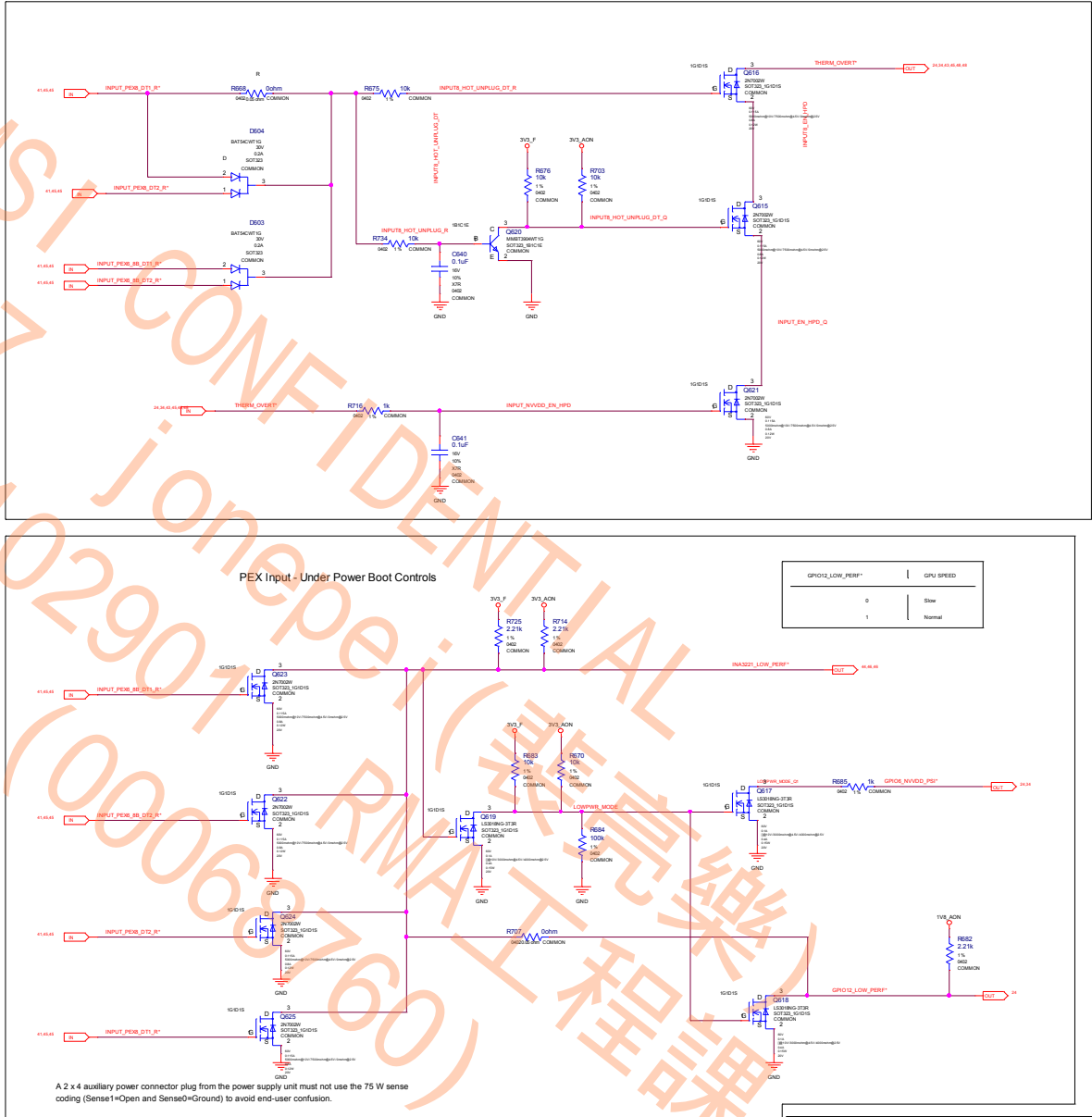
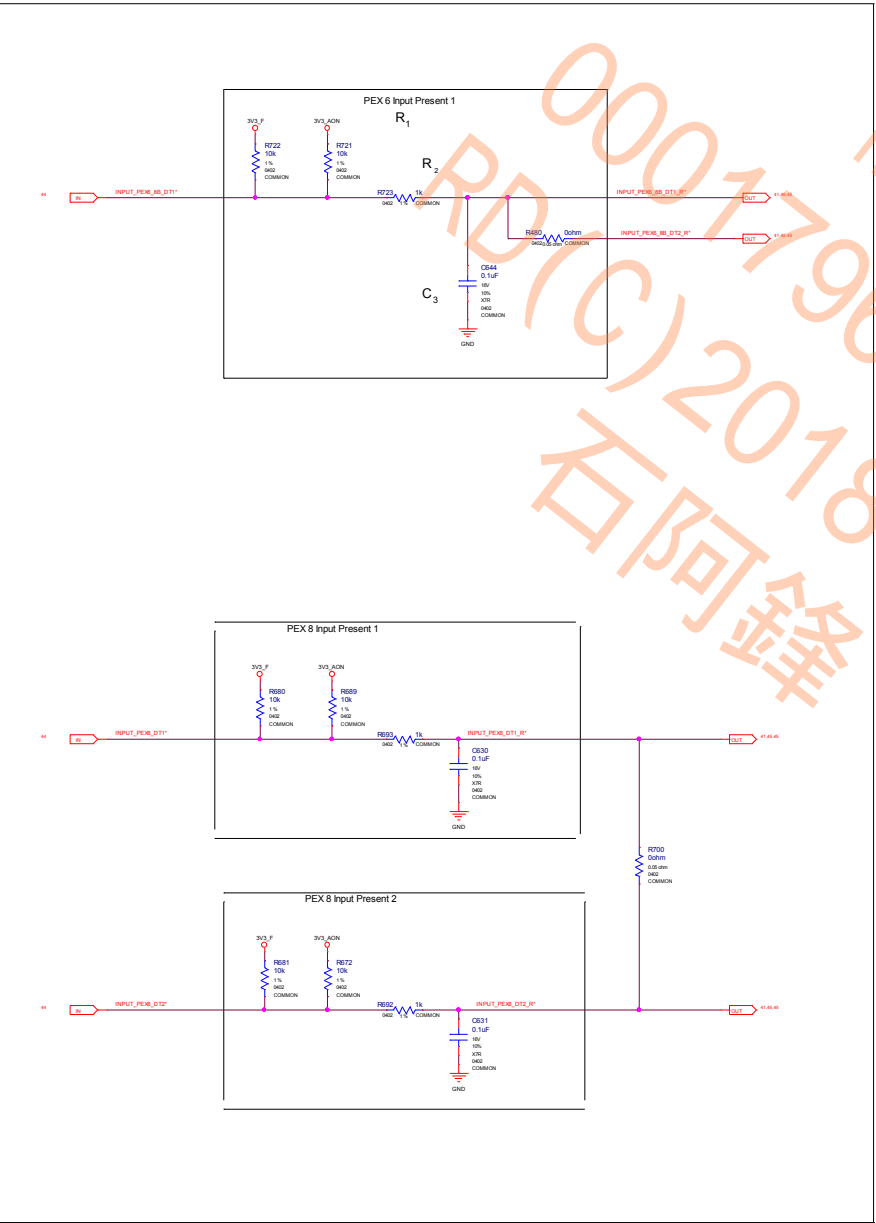


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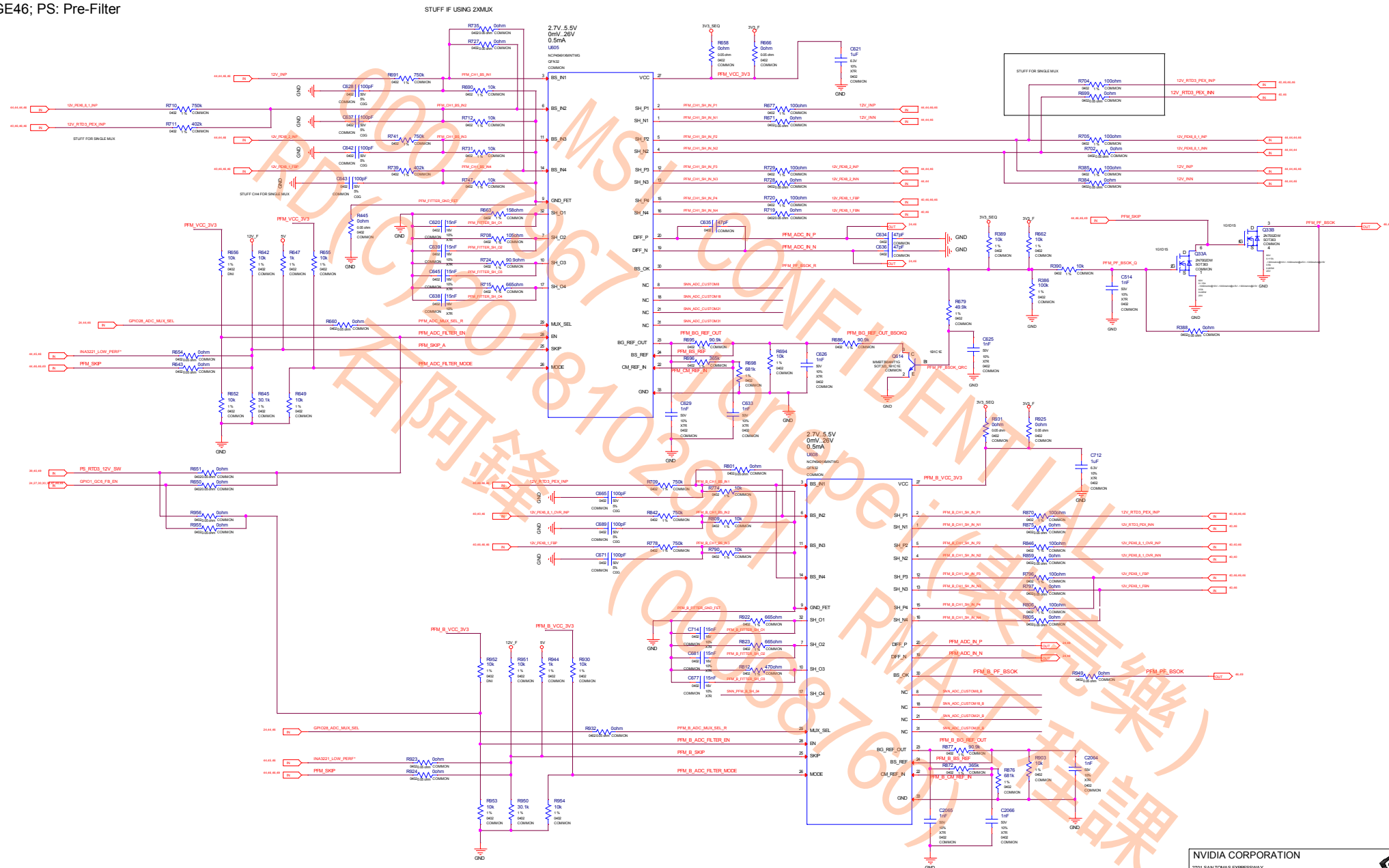




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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	PS: CURRENT STEERING, HOT UNPLUG DETECT

NVIDIA CORPORATION			
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PRE-FILTER

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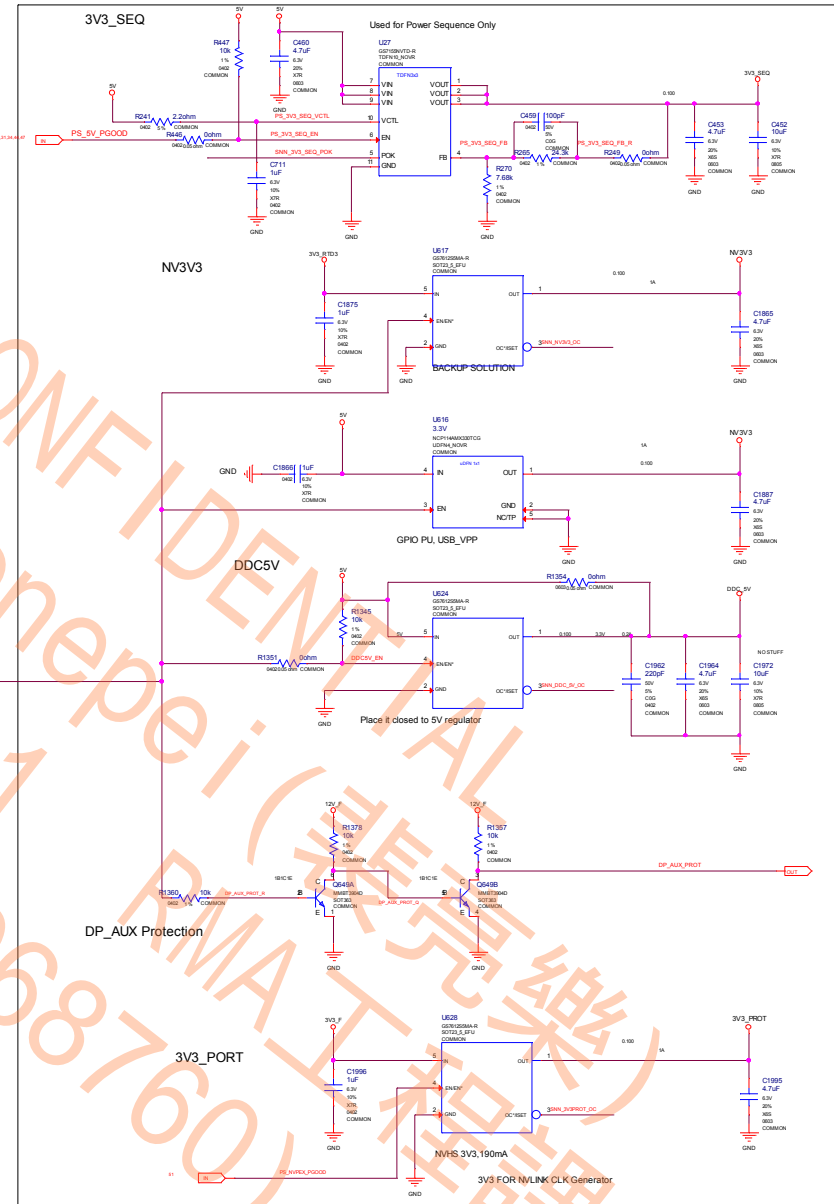


NV_PN	600-1G180-BASE-200
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQUENCE: 5V, 1V8, NV3V3 ENABLE

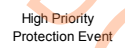
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NV_PN	600-1G180-BASE-200
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PCB REV	PG180-A02
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BOM REV	A	DATE	27-JUN-2018
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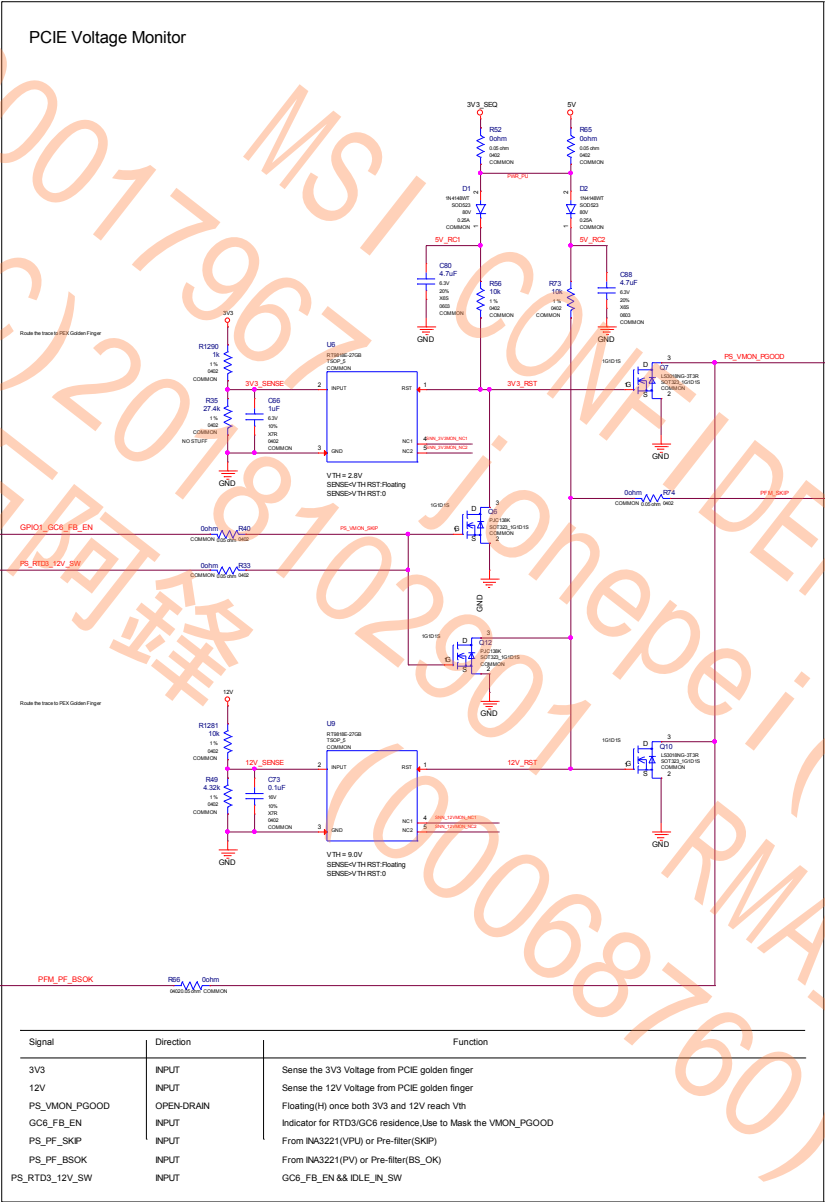
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PEX ENABLE

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BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ
Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX
and All Input 12Vs

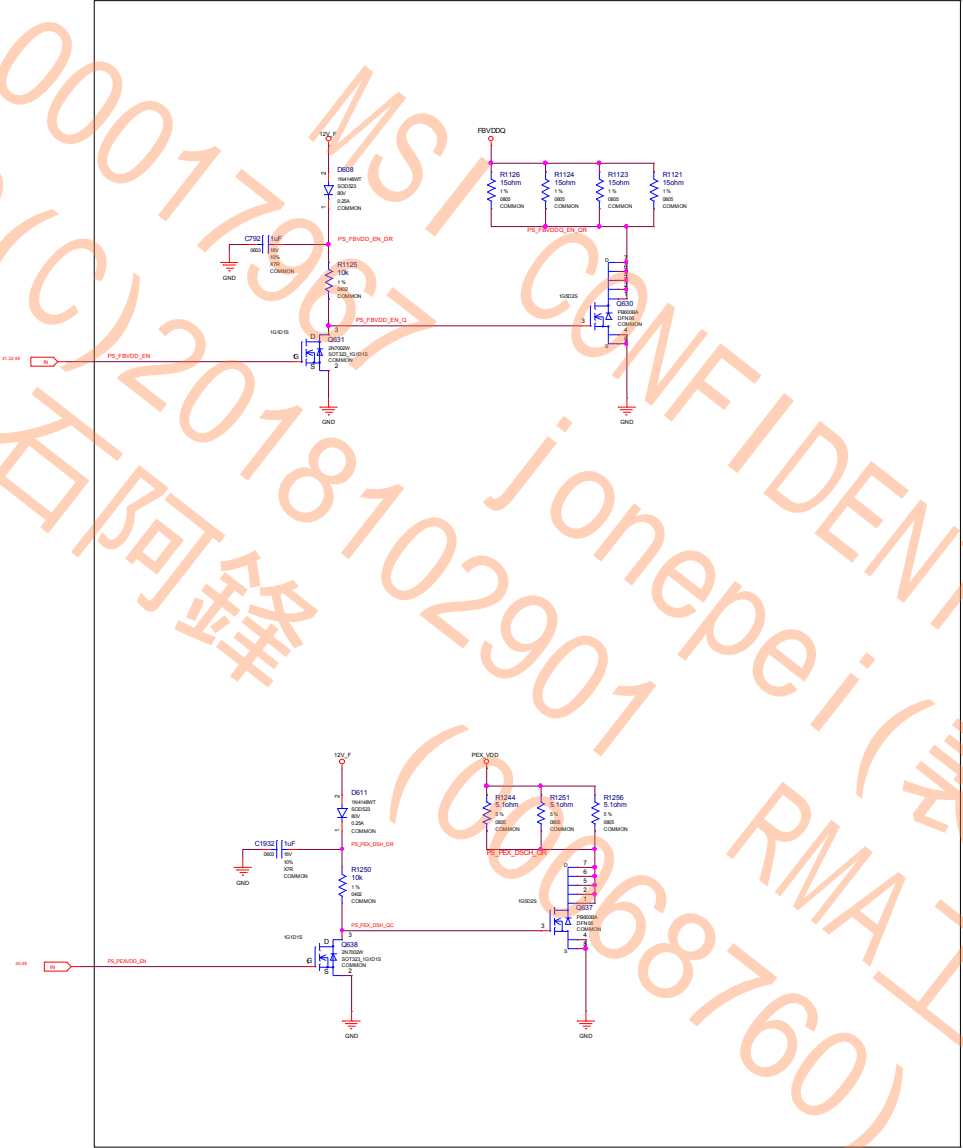
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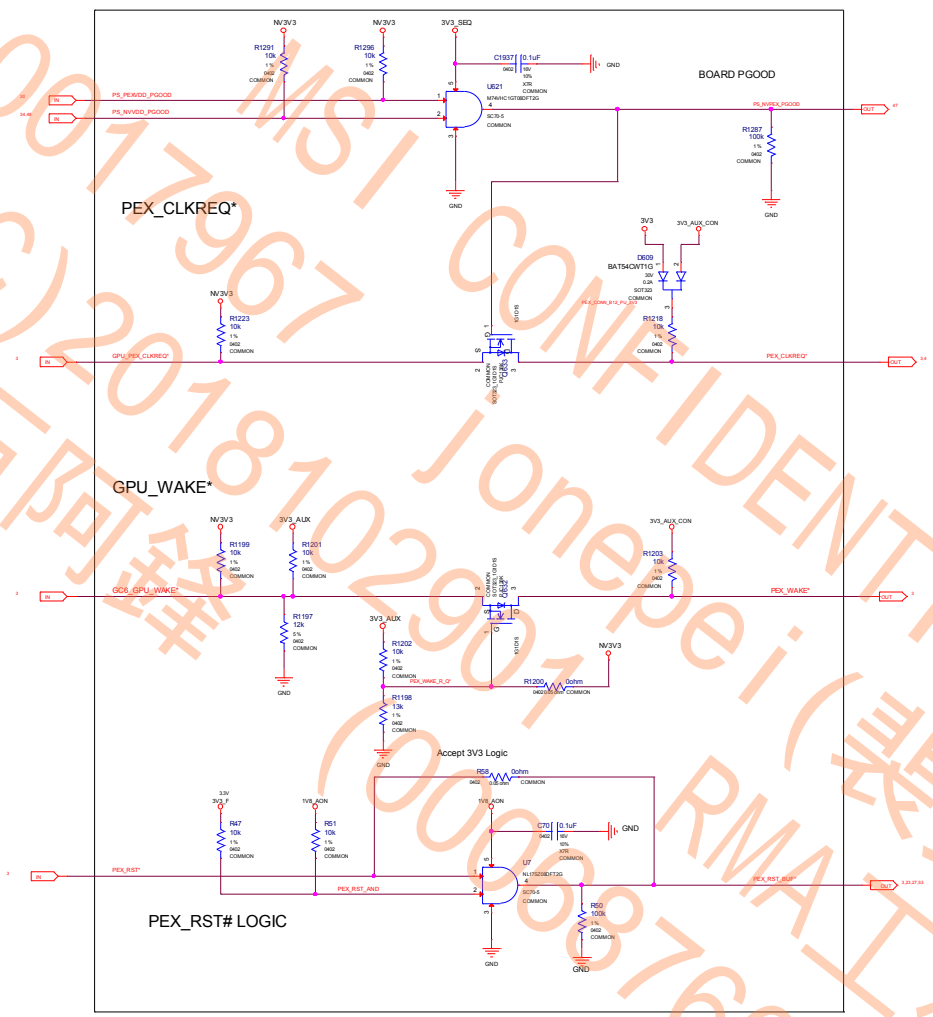
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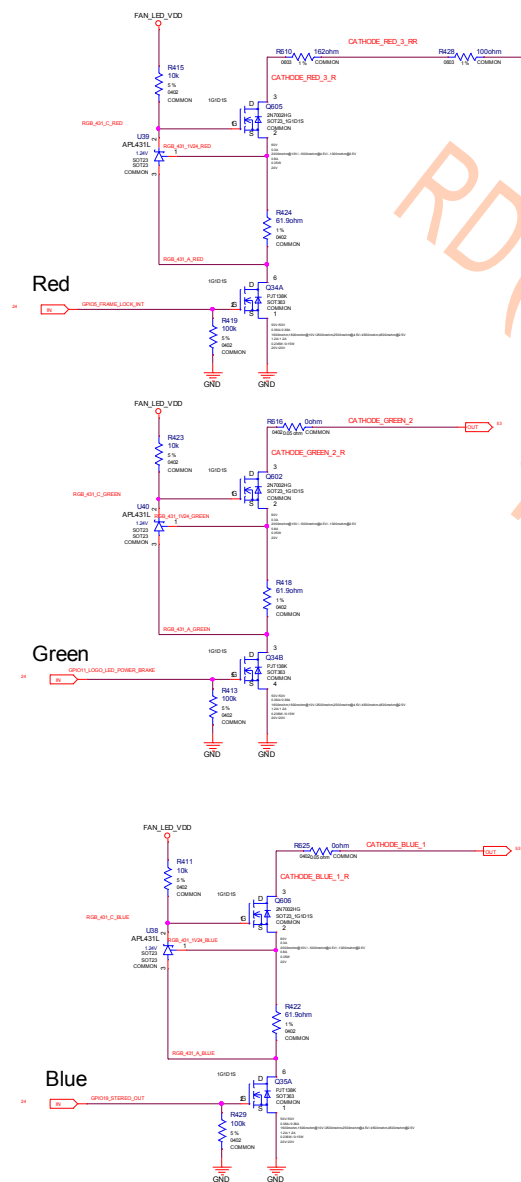
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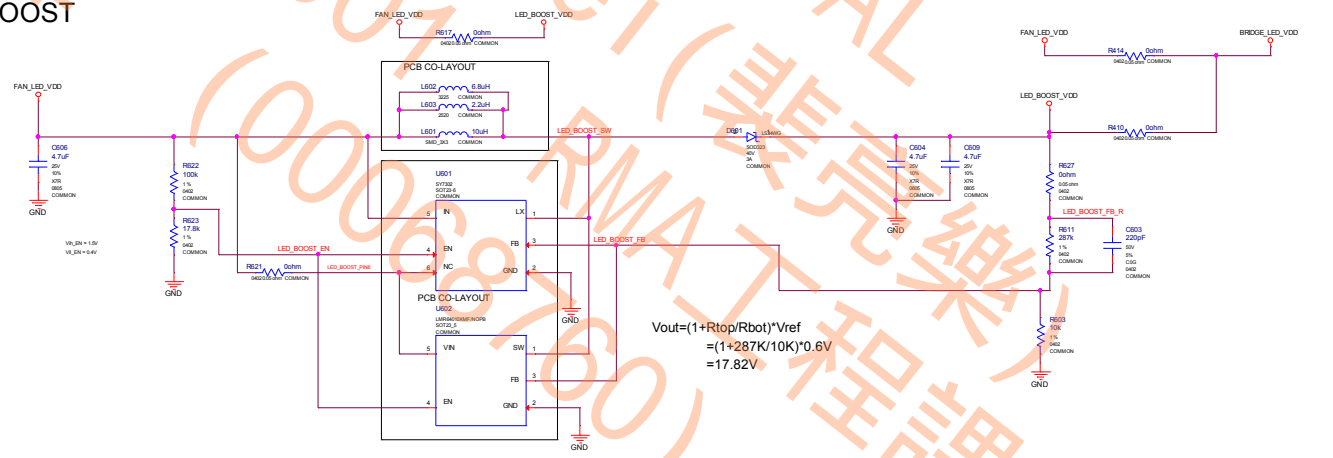


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			<div> <div>PAGE</div> <div>51 OF 54</div> </div>

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LED BOOST



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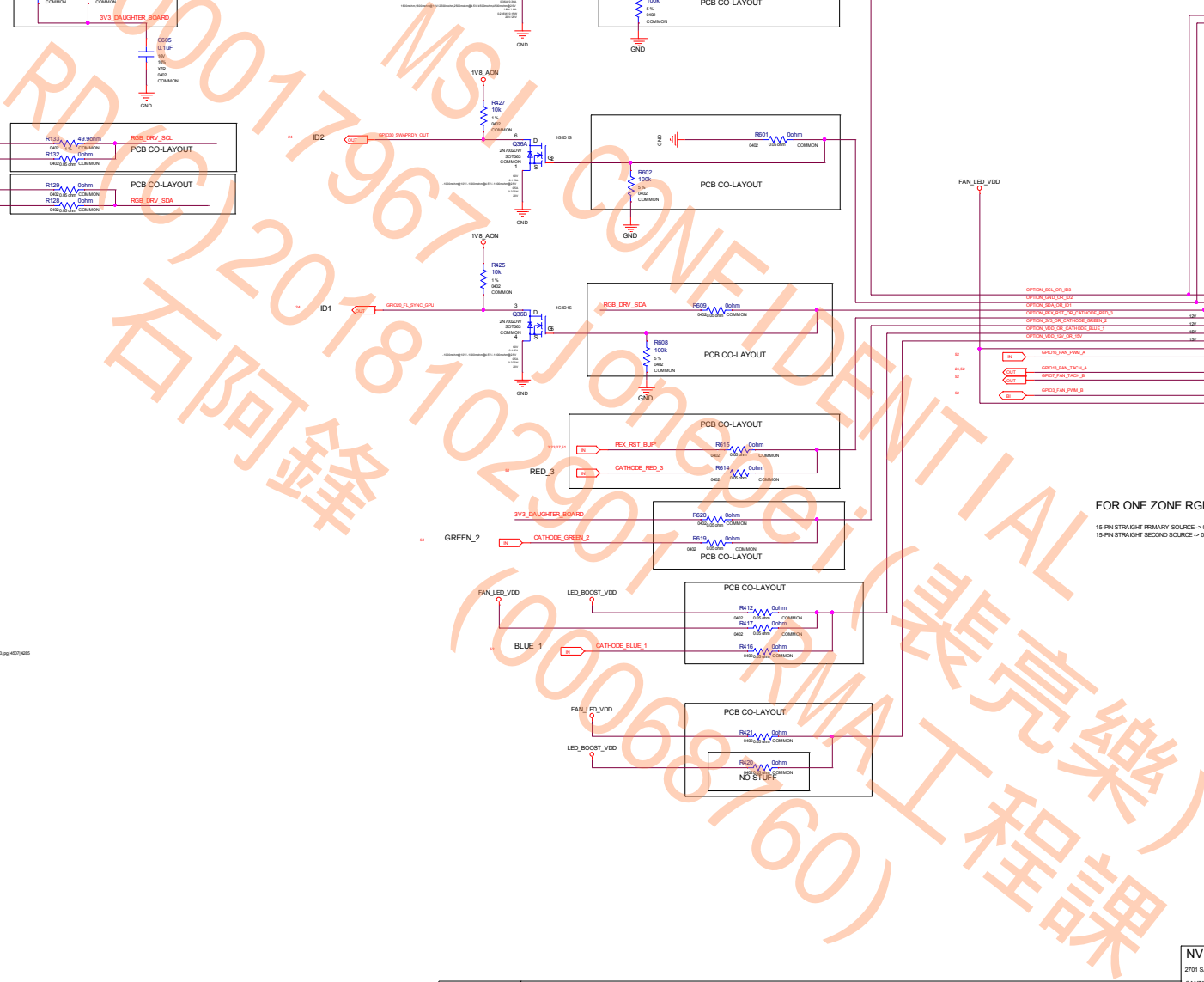
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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	LED & FAN HEADERS

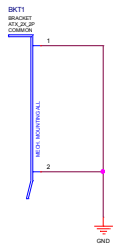
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Brackets:



Bracket Screw

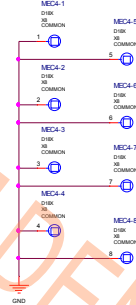


BOARD STIFFENER

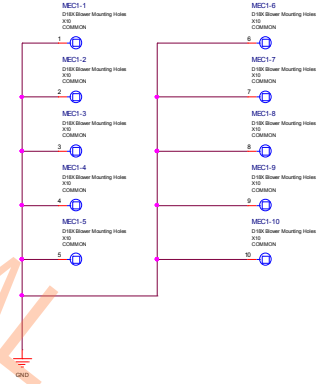


STIFFENER

GPU Mounting holes



Mechanical Holes Symbol



GPU Socket Symbol



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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	Mechanical Bracket/Thermal Solution

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